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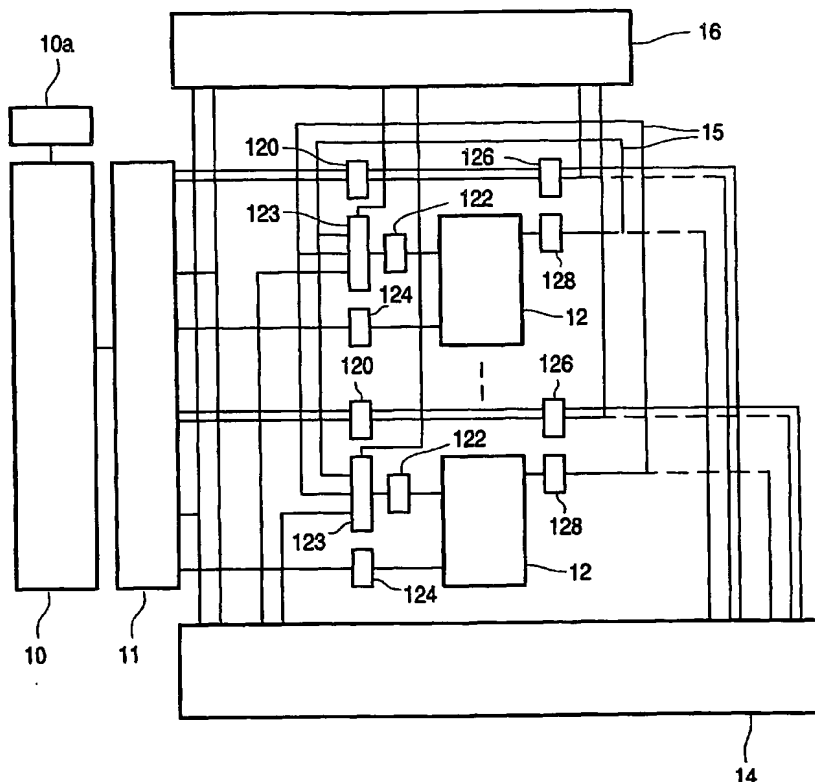
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(54) Title: USE OF BYPASSING IN A PIPELINED INSTRUCTION PROCESSOR



(57) Abstract: An instruction processing device has a of pipe-line stage with a functional unit for executing a command from an instruction. A first register unit is coupled to the functional unit for storing a result of execution of the command when the command has reached a first one of the pipeline stages, and for supplying bypass operand data to the functional unit. A register file is coupled to the functional unit for storing the result when the command has reached a second one of the pipeline stages, downstream from the first one of the pipeline stages, and for supplying operand data to the functional unit. A disable circuit is coupled to selectively disable storing of the results in the register file under control of the instructions.



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